HC55185 and the IDT821068 Programmable Octal PCM CODEC

Application Note | December 2001 | AN9947.1

Author: Don LaFontaine

Reference Design using the HC55185 and the IDT821068 Programmable Octal PCM CODEC

The purpose of this application note is to provide a reference design for the HC55185 and IDT821068 Programmable Octal PCM CODEC.

The network requirements of many countries require the analog subscriber line circuit (SLIC) to terminate the subscriber line with an impedance for voiceband frequencies which is complex, rather than resistive (e.g. 600Ω). The HC55185 accomplishes this impedance matching with a single network connected between the VTX pin and the -IN pin.

The IDT821068 Octal PCM CODEC uses an integrated programmable DSP to realize AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions.

Discussed in this application note are the following:

- 2-wire impedance matching
- Receive gain (4-wire to 2-wire) and transmit gain (2-wire to 4-wire) calculations
- Reference design for both 600Ω and 200Ω +680Ω||0.1µF (China Complex Impedance)

Impedance Matching

Impedance matching of the HC55185 to the subscriber load is important for optimization of 2-wire return loss, which in turn cuts down on echoes in the end to end voice communication path. Impedance matching of the HC55185 is accomplished by making the SLIC's impedance (Z_O, Figure 1) equal to the desired terminating impedance Z_L, minus the value of the protection resistors (R_P).

With the HC55185 programmed to match a ZL of 600Ω, the IDT821068 uses an integrated programmable DSP to realize any AC impedance. The formula to program the HC55185 to match a 2-wire impedance of 600Ω is shown in Equation 1.

$$R_S = 133.3 \bullet (Z_L - 2R_P) = 133.3 \bullet (600\Omega - 2R_P) \quad \text{(EQ. 1)}$$

The value of R_S with 49Ω protection resistors is 66.9kΩ. The closest standard value is 66.5kΩ.

SLIC in the Active Mode

Figure 2 shows a simplified AC transmission model of the HC55185 and the connection of the IDT821068 to the SLIC. Circuit analysis of the HC55185 yields the following design equations:

The Sense Amplifier is configured as a 4 input differential amplifier with a gain of 3/4. The voltage at the output of the sense amplifier (V_{SA}) is calculated using superposition. $V_{SA}1$ is the voltage resulting from V1, $V_{SA}2$ is the voltage resulting from V2 and so on (reference Figure 2).

$$V_{SA}1 = -\frac{3}{4}(V_1) \quad \text{(EQ. 2)}$$

$$V_{SA}2 = \frac{3}{4}(V_2) \quad \text{(EQ. 3)}$$

$$V_{SA}3 = -\frac{3}{4}(V_3) \quad \text{(EQ. 4)}$$

$$V_{SA}4 = \frac{3}{4}(V_4) \quad \text{(EQ. 5)}$$

$$V_{SA} = [(V_2 - V_1) + (V_4 - V_3)]\frac{3}{4} = [\Delta V + \Delta V]\frac{3}{4} \quad \text{(EQ. 6)}$$

Where ΔV is equal to $I_M R_{SENSE}$ (R_{SENSE} = 20Ω)

$$V_{SA} = 2(\Delta I_M \times 20)\frac{3}{4} = \Delta I_M 30 \quad \text{(EQ. 7)}$$

The voltage at VTX is equal to:

$$V_{TX} = -V_{SA}\left(\frac{R_S}{8K}\right) = -\left(\frac{R_S}{8K}\right)\Delta I_M 30 \quad \text{(EQ. 8)}$$

V_{TR} is defined in Figure 2, note polarity assigned to V_{TR}:

$$V_{TR} = 2(V_{RX} + V_{TX}) \quad \text{(EQ. 9)}$$

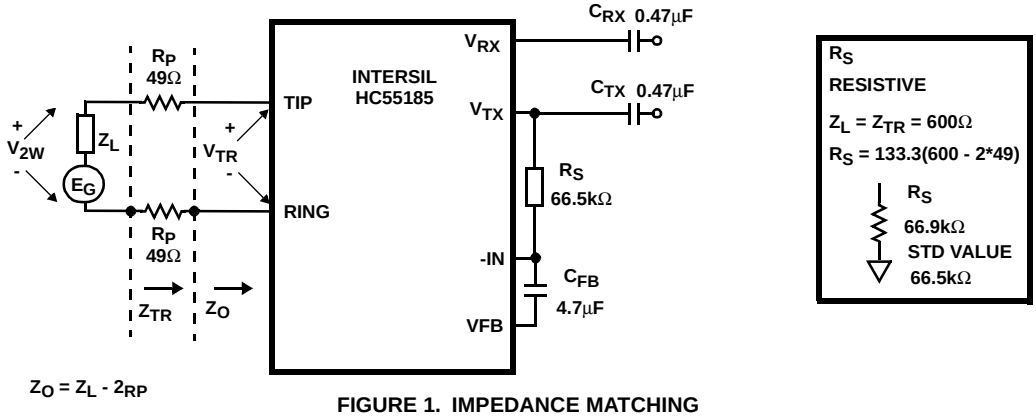


FIGURE 1. IMPEDANCE MATCHING

Setting V_{RX} equal to zero, substituting Equation 8 into Equation 9 and defining $Z_O = -V_{TR}/\Delta I_M$ will enable the user to determine the require feedback to match the line impedance at V_{2W}.

$$Z_O = \frac{1}{133.33} R_S \quad \text{(EQ. 10)}$$

Z_O is the source impedance of the device and is defined as $Z_O = Z_L - 2R_p$. ZL is the line impedance. R_S is defined as:

$$R_S = 133.33(Z_L - 2R_P) \quad \text{(EQ. 11)}$$

Node Equation at HC55185 V_{RX} input

$$I_X = \frac{V_{RX}}{R} + \frac{V_{TX}}{R} \quad \text{(EQ. 12)}$$

Substitute Equation 8 into Equation 12

$$I_X = \frac{V_{RX}}{R} - \left(\frac{R_S \Delta I_M 30}{R 8K}\right) \quad \text{(EQ. 13)}$$

Loop Equation at HC55185 feed amplifiers and load

$$I_X R - V_{TR} + I_X R = 0 \quad \text{(EQ. 14)}$$

Substitute Equation 13 into Equation 14

$$V_{TR} = 2V_{RX} - \left(\frac{R_S \Delta I_M 60}{8K}\right) \quad \text{(EQ. 15)}$$

Substitute Equation 10 for R_S and $-V_{2W}/Z_L$ for ΔI_M into Equation 15.

$$V_{TR} = 2V_{RX} + \frac{Z_O V_{2W}}{Z_L} \quad \text{(EQ. 16)}$$

Loop Equation at Tip/Ring interface

$$V_{2W} - I_M 2R_P + V_{TR} = 0 \quad \text{(EQ. 17)}$$

Substitute Equation 16 into Equation 17 and combine terms

$$V_{2W}\left[\frac{Z_L + Z_O + 2R_P}{Z_L}\right] = -2V_{RX} \quad \text{(EQ. 18)}$$

where:

V_{RX} = The input voltage at the V_{RX} pin.

V_{SA} = An internal node voltage that is a function of the loop current and the output of the Sense Amplifier.

I_X = Internal current in the SLIC that is the difference between the input receive current and the feedback current.

I_M = The AC metallic current.

R_P = A protection resistor (typical 49.9Ω).

R_S = An external resistor/network for matching the line impedance.

V_{TR} = The tip to ring voltage at the output pins of the SLIC.

V_{2W} = The tip to ring voltage including the voltage across the protection resistors.

Z_L = The line impedance.

Z_O = The source impedance of the device.

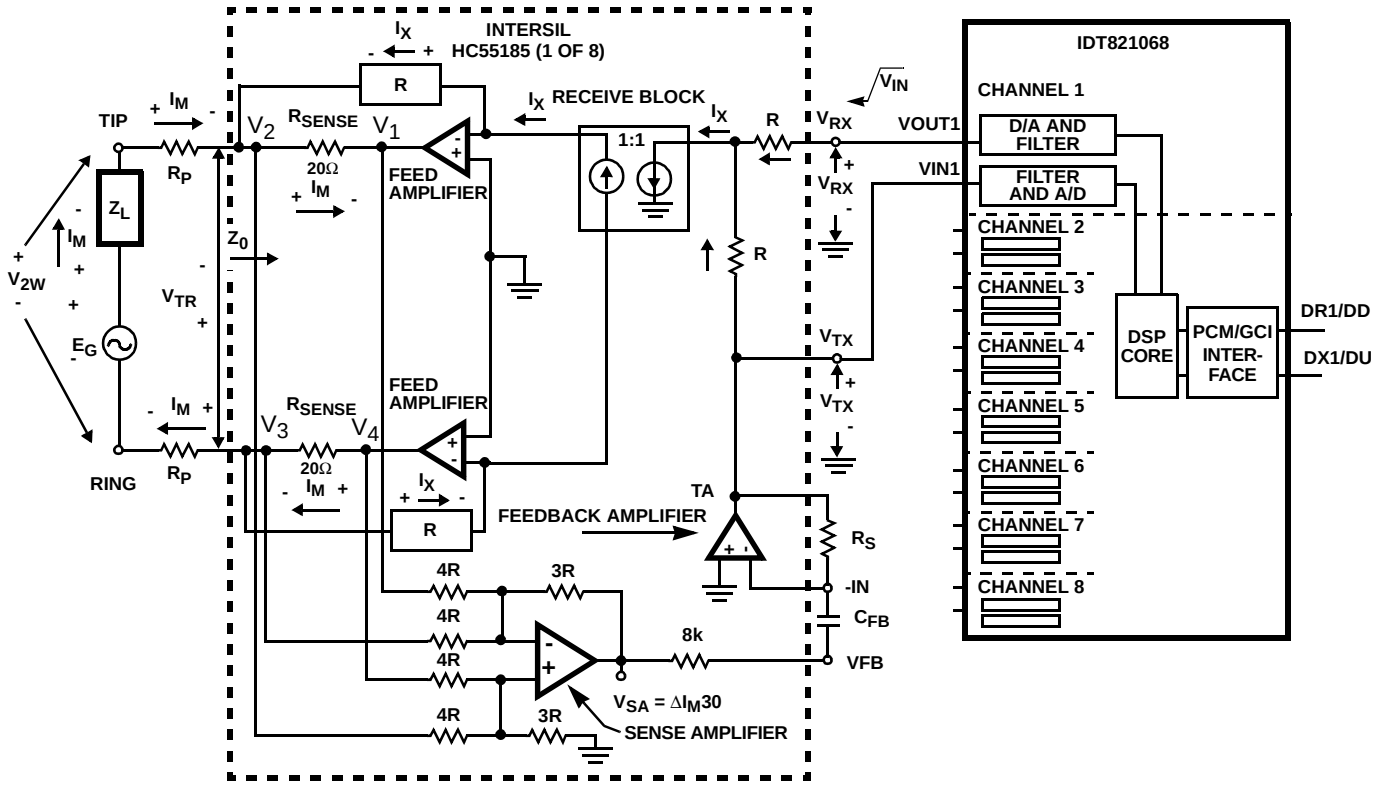


FIGURE 2. HC55185 SIMPLIFIED AC TRANSMISSION CIRCUIT AND IDT821068

HC55185 Receive Gain (V_{RX} to V_{2W})

4-wire to 2-wire gain across the HC55185 is equal to the V_{2W} divided by the input voltage V_{RX}, reference Figure 2. The receive gain is calculated using Equation 18.

Equation 19 expresses the receive gain (V_{RX} to V_{2W}) in terms of network impedances. From Equation 11, the value of R_S was set to match the line impedance (Z_L) to the HC55185 plus the protection resistors ($Z_0 + R_P$). This results in a 4-wire to 2-wire gain of -1, as shown in Equation 19.

$$G_{4\text{-}2} = \frac{V_{2W}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_O + 2_{RP}} = -2\frac{Z_L}{Z_L + Z_L} = -1 \quad \text{(EQ. 19)}$$

Receive Gain Across the System

The receive gain across the system is defined as the gain from the PCM highway to the phone (V_{2W}). With the receive gain through the HC55185 set to 1, the receive gain across the system is entirely controlled by programming the IDT821068. The IDT821068 can program the receive gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog receive gain, also known as Digital to Analog (D/A) gain, can be programmed in the IDT821068 to be either 0dB or -6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the receive path can be programmed from +6 to -12dB with minimum 0.1dB steps.

This results in a possible receive gain (D/A) programming range from +6dB to -18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821068 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

Transmit Gain Across HC55185 (E_G to V_{TX})

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with $V_{RX} = 0$, reference Figure 2.

Loop Equation

$$-E_G + Z_L I_M + 2R_P I_M - V_{TR} = 0 \quad \text{(EQ. 20)}$$

From Equation 16 with $V_{RX} = 0$

$$V_{TR} = \frac{Z_O V_{2W}}{Z_L} \quad \text{(EQ. 21)}$$

Substituting Equation 21 into Equation 20 and simplifying.

$$E_G = -V_{2W}\left[\frac{Z_L + 2R_P + Z_O}{Z_L}\right] \quad \text{(EQ. 22)}$$

Substituting Equation 10 into Equation 8 and defining $\Delta I_M = -V_{2W}/Z_L$ results in Equation 23 for VTX.

$$_{TX} = \frac{V_{2W}}{2}\left[\frac{Z_L - 2R_P}{Z_L}\right] \quad \text{(EQ. 23)}$$

Combining Equations 22 and 23 results in Equation 24.

$$G_{2\text{-}4} = \frac{V_{TX}}{E_G} = -\frac{Z_L - 2R_P}{2(Z_L + 2R_P + Z_O)} = -\frac{Z_O}{2(Z_L + 2R_P + Z_O)} \quad \text{(EQ. 24)}$$

A more useful form of the equation is rewritten in terms of V_{TX}/V_{2W}. A voltage divider equation is written to convert from E_G to V_{2W} as shown in Equation 25.

$$V_{2W} = \left(\frac{Z_O + 2_{RP}}{Z_L + Z_O + 2_{RP}}\right)E_G \quad \text{(EQ. 25)}$$

Substituting $Z_L = Z_O + 2_{RP}$ and rearranging Equation 25 in terms of E_G results in Equation 26.

$$E_G = 2V_{2W} \quad \text{(EQ. 26)}$$

Substituting Equation 26 into Equation 24 results in an equation for 2-wire to 4-wire gain that’s a function of the synthesized input impedance of the SLIC and the protection resistors.

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{2W}} = -\frac{Z_O}{(Z_L + 2R_P + Z_O)} = 0.416 \quad \text{(EQ. 27)}$$

Z_L is set to 600Ω, Z_O is programmed with R_S to be 498.76Ω (66.5kΩ/133.33), and R_P is equal to 49.9Ω. This results in a 2-wire to 4-wire gain of 0.416 or -7.6dB.

Transmit Gain Across the System

The transmit gain across the system is defined as the gain from the phone or 2-wire side (V_{2W}) to the PCM highway. Setting the gain of the IDT821068 will have to account for the attenuated signal through the HC55185. The system gain is entirely controlled by programming the IDT821068. The IDT821068 can program the transmit gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog transmit gain, also known as Analog to Digital (A/D) gain, can be programmed in the IDT821068 to be either 0dB or +6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the transmit path can be programmed from -6dB to +12dB with minimum 0.1dB steps.

This results in a possible transmit gain (A/D) programming range from -6dB to +18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821068 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

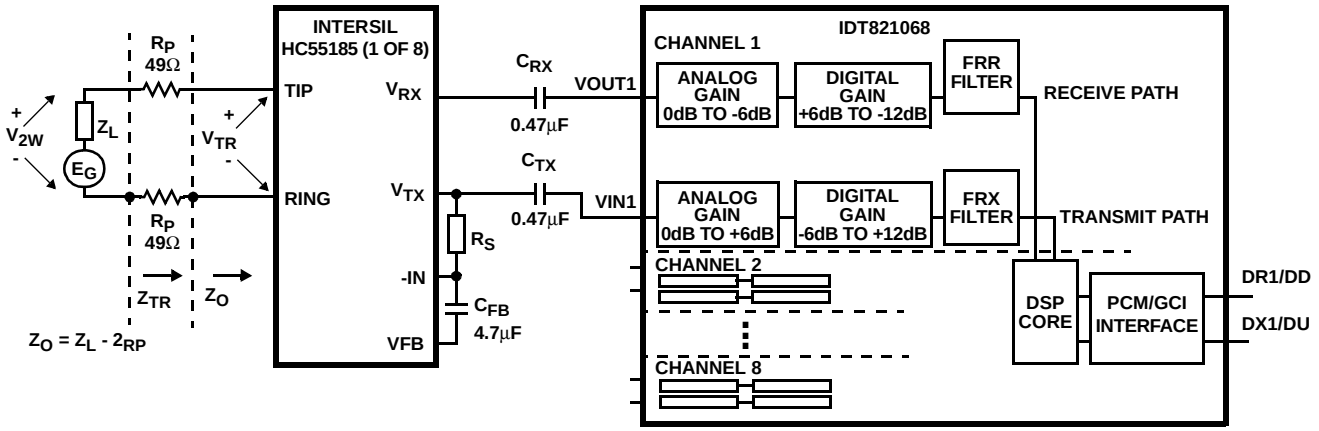


FIGURE 3. RECEIVE GAIN G(4-2), TRANSMIT GAIN (2-4)

Transhybrid Balance G(4-4)

Transhybrid balance is a measure of how well the input signal is canceled (that being received by the SLIC) from the transmit signal (that being transmitted from the SLIC to the CODEC). Without this function, voice communication would be difficult because of the echo. The Transhybrid balancing filter inside the IDT821068 is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation is ECF.

Frequency Response Correction

The FRR filter in the receive path and the FRX filter in the transmit path can be programmed to correct any frequency distortion caused by the impedance matching filters. The coefficients of Frequency Response Correction are FRR for receive path and FRX for the transmit path.

Information Required for IDT to Calculate IDT821068 CODEC DSP Coefficients

For IDT to calculate IDT821068 DSP coefficient, customers should provide the following information about their subscriber line card:

- Accurate SLIC PSPICE model. It can be provided in .lib file or PSPICE schematic file.
- System Impedance
- Gain (Transmit path and Receive path)

Using the DSP coefficients provided by IDT, the overall performance of the system will pass ITU-T requirements.

When the COF RAM button is selected from the MPI Operation General Interface screen, the COF RAM Operation screen will appear (Figure 4). From this screen, the user can configure all the coefficients for the current channel.

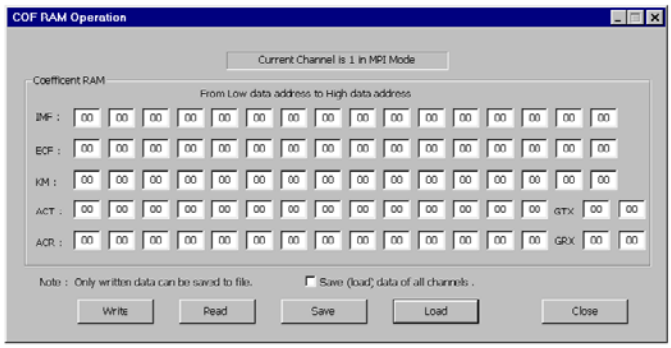


FIGURE 4. COEFFICIENT RAM OPERATION SCREEN

Reference Design of the HC55185 and the IDT821068 With a 600Ω Load

The design criteria is as follows:

- 4-wire to 2-wire gain (DR1/DD to V_{2W}) equal 0dB
- 2-wire to 4-wire gain (V_{2W} to DX1/DU) equal 0dB
- Rp = 49.9Ω

Figure 5 gives the reference design using the Intersil HC55185 and the IDT821068 Programmable Octal PCM CODEC. Also shown in Figure 5 are the voltage levels at specific points in the circuit.

Impedance Matching

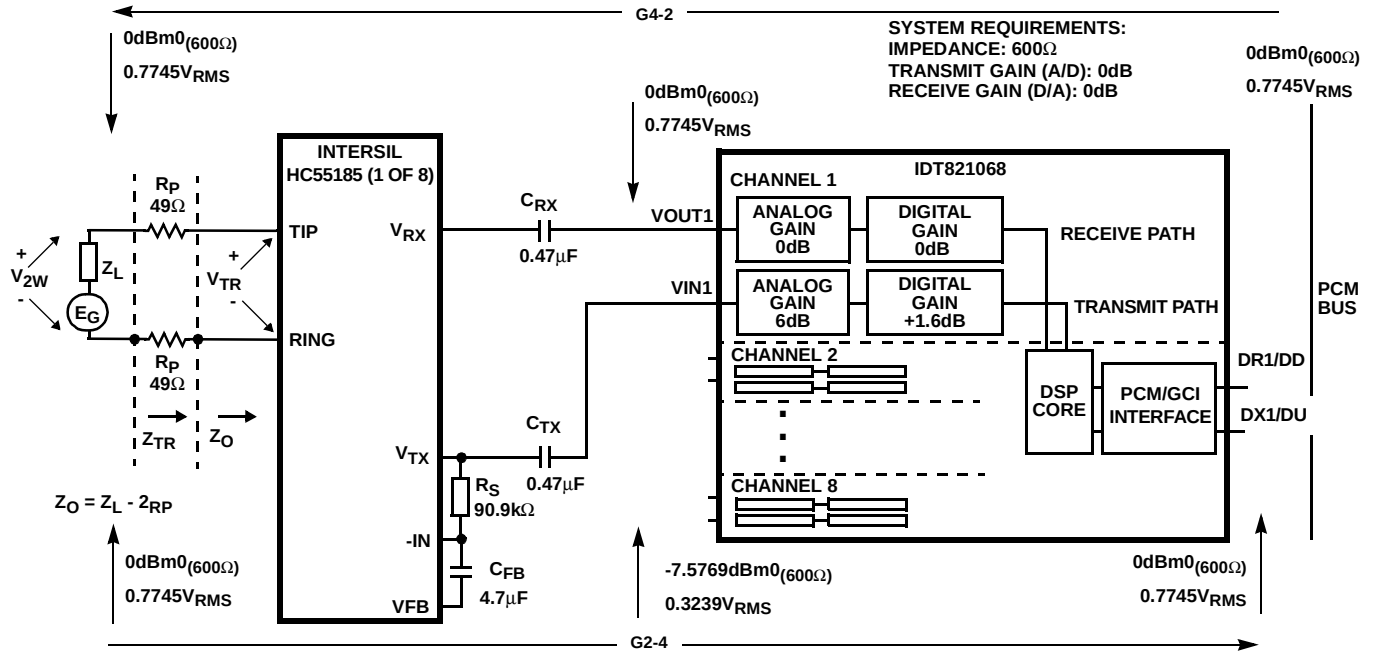
The 2-wire impedance is matched to the line impedance Z_0 using Equation 1, repeated here in Equation 28.

$$R_S = 133.3 \bullet (Z_L - 2R_P) \quad \text{(EQ. 28)}$$

For a line impedance of 600Ω, R_S equals:

$$R_S = 133.3 \bullet (600 - 98) = 66.9k\Omega \quad \text{(EQ. 29)}$$

The closest standard value for R_S would be 66.5kΩ.



NOTE: Reference Table 1 for coefficients.

FIGURE 5. REFERENCE DESIGN OF THE HC55185 AND THE IDT821068 WITH A 600Ω LOAD IMPEDANCE

However, it would be very convenient and cost effective if system manufacturers can use only one type of line card to meet different impedance requirements and different gain requirements. The programmability of IDT821068 can help system manufactures to reach this goal. By using different coefficients and tweaking the value of R_S, this reference design can meet both 600Ω and 200Ω + 680Ω||0.1μF impedance requirements. To obtain the best results, R_S should be an optimized value. By experimental experience, it is recommended to set R_S = 90.9kΩ ± 1%

With the optimized value of R_S selected to be 90.9kΩ ± 1%, the coefficients for different Transmit Gains (A/D) and Receive Gains (with a line impedance of 600Ω) are given in Tables 1, 2 and 3.

Although the impedance matching resistor (R_S) of the HC55185 has been changed, the contribution from the IDT821068 allows the system to still match the load. With the load matched, the 2-wire to 4-wire gain (Equation 27) is still equal to -7.6dB.

Specific Implementation for China

The design criteria for a China specific solution are as follows:

- Desired line circuit impedance is 200 + 680//0.1μF
- Receive gain (V_{2W}/(DR1/DD)) is -3.5dB
- Transmit gain ((DX1/DU)/V_{2W}) is 0dB
- 0dBm0 is defined as 1mW into the complex impedance at 1020Hz
- R_p = 49.9Ω

Figure 6 gives the reference design using the Intersil HC55185 and the IDT821068 Programmable Octal PCM CODEC. Also shown in Figure 6 are the voltage levels at specific points in the circuit. Note: The transmit gain of the system is 0dB (-2.19dB$_{(811Ω)}$ = -3.5dB$_{(600Ω)}$) as explained in the following section.

Adjustment to Get -3.5dBm0 at the Load Referenced to 600Ω

The voltage equivalent to 0dBm0 into 811Ω (0dBm0$_{(811Ω)}$) is calculated using Equation 30 (811Ω is the impedance of complex China load at 1020Hz).

$$0dBm_{(811\Omega)} = 10\log\frac{V^2}{811(0.001)} = 0.90055V_{RMS} \quad \text{(EQ. 30)}$$

The gain referenced back to 0dBm0$_{(600Ω)}$ is equal to:

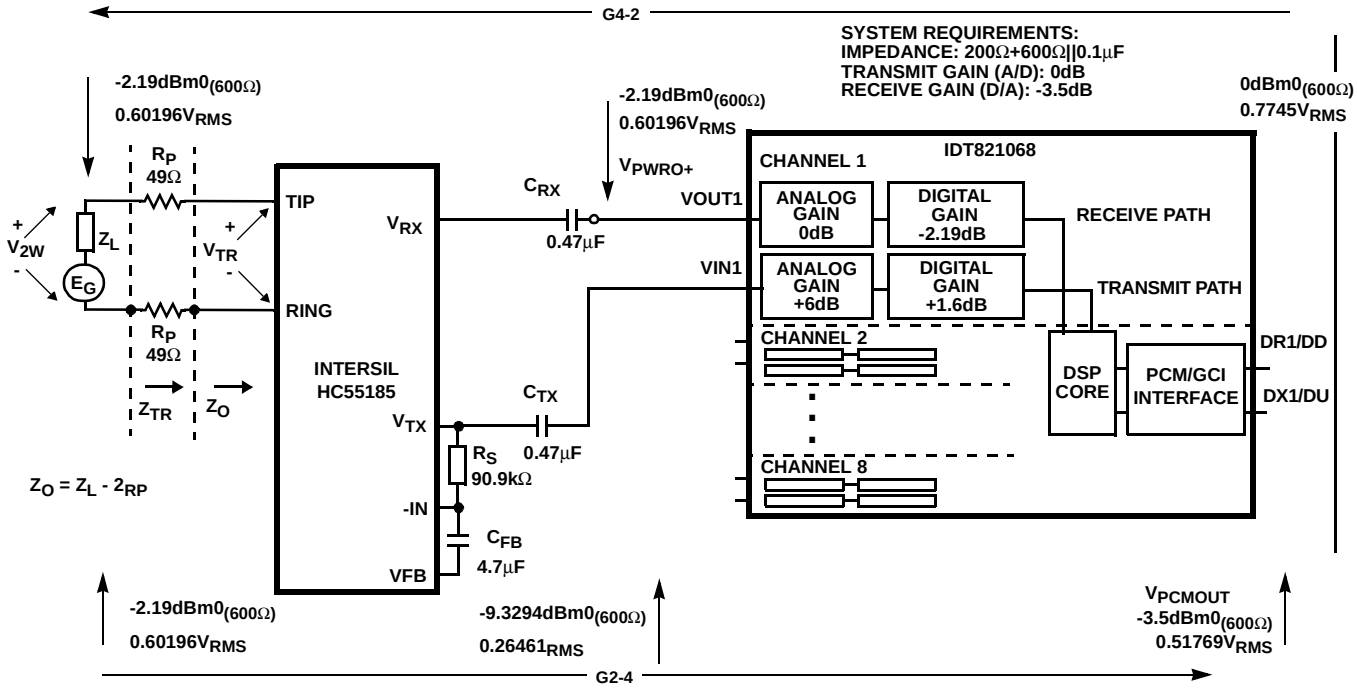
$$GAIN = 20\log\frac{0.90055V_{RMS}}{0.7745V_{RMS}} = 1.309dB \quad \text{(EQ. 31)}$$

The adjustment to get -3.5dBm0 at the load referenced to 600Ω is:

$$Adjustment = -3.5dBm0 + 1.309dBm0 = -2.19dB \quad \text{(EQ. 32)}$$

The voltage at the load (referenced to 600Ω) is given in Equation 33:

$$-2.19dBm_{(600\Omega)} = 10\log\frac{V^2}{600(0.001)} = 0.60196V_{RMS} \quad \text{(EQ. 33)}$$



NOTE: Reference Table 5 for coefficients.

FIGURE 6. REFERENCE DESIGN OF THE HC55185 AND THE IDT821068 WITH CHINA COMPLEX LOAD IMPEDANCE

Impedance Matching

With the optimized value of R_S selected to be 90.9kΩ ± 1%, the coefficients for different Transmit Gains (A/D) and Receive Gains (with a line impedance of 200Ω + 680Ω||0.1μF) are given in Tables 4, 5 and 6.

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

COEFFICIENT RAM				CHANNEL 1													
IMF:	43	FD	90	EC	92	26	8A	EF	FF	7F	00	00	00	00	00	00	
ECF:	FB	00	8F	FF	97	FE	5A	07	23	1B	C1	1E	2F	F9	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	DD	FF	33	FE	AD	42	AD	42	33	FE	DD	FF	CD	AC	***GTX***	FF	1F
ACR:	BF	00	36	FD	6A	42	6A	42	36	FD	BF	00	01	88	***GRX***	FA	02
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	6C	FC	85	EE	1A	25	E3	EF	FF	7F	00	00	00	00	00	00	
ECF:	9D	00	F5	FF	1F	FF	9C	04	AD	1A	7C	23	9F	F7	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	8C	FF	6D	FE	8C	42	8C	42	6D	FE	8C	FF	CD	C0	***GTX***	A1	1F
ACR:	E6	00	EA	FC	94	42	94	42	EA	FC	E6	00	01	88	***GRX***	F1	02
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	69	FD	BB	EB	DB	27	FB	EE	FE	7F	00	00	00	00	00	00	
ECF:	BE	01	CD	FE	30	FF	62	02	28	19	76	2C	26	F3	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	C5	FF	CF	FD	01	43	01	43	CF	FD	C5	FF	CD	AC	***GTX***	A1	1F
ACR:	E8	00	92	FC	DC	42	DC	42	92	FC	E8	00	01	88	***GRX***	FA	02

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

COEFFICIENT RAM				CHANNEL 4													
IMF:	2F	FD	EC	EB	2A	28	B5	EE	FF	7F	00	00	00	00	00	00	
ECF:	35	01	70	FF	B0	FF	8C	00	F1	17	41	31	44	F1	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	C3	FF	AB	FD	1A	43	1A	43	AB	FD	C3	FF	CD	AC	***GTX***	A1	1F
ACR:	0C	01	29	FC	1D	43	1D	43	29	FC	0C	01	01	88	***GRX***	FA	02
COEFFICIENT RAM				**CHANNEL 5**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	ED	FF	79	FD	2E	43	2E	43	79	FD	ED	FF	CD	AC	***GTX***	A1	1F
ACR:	1A	01	24	FC	22	43	22	43	24	FC	1A	01	01	88	***GRX***	F1	02
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	B2	FF	64	FD	5A	43	5A	43	64	FD	B2	FF	CD	AC	***GTX***	FF	1F
ACR:	39	01	BC	FB	72	43	72	43	BC	FB	39	01	01	88	***GRX***	F1	02
COEFFICIENT RAM				**CHANNEL 7**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	AB	FF	46	FD	77	43	77	43	46	FD	AB	FF	CD	AC	***GTX***	FF	1F
ACR:	3C	01	66	FB	A9	43	A9	43	66	FB	3C	01	01	88	***GRX***	F1	02
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	77	FF	32	FD	C1	43	C1	43	32	FD	77	FF	CD	AC	***GTX***	FF	1F
ACR:	2A	01	2C	FB	DE	43	DE	43	2C	FB	2A	01	01	88	***GRX***	FA	02

TABLE 2. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-3.5dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

COEFFICIENT RAM				CHANNEL 1													
IMF:	43	FD	90	EC	92	26	8A	EF	FF	7F	00	00	00	00	00	00	
ECF:	FB	00	8F	FF	97	FE	5A	07	23	1B	C1	1E	2F	F9	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	DD	FF	33	FE	AD	42	AD	42	33	FE	DD	FF	CD	AC	***GTX***	FF	1F
ACR:	BF	00	36	FD	6A	42	6A	42	36	FD	BF	00	01	88	***GRX***	FD	01

TABLE 2. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-3.5dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

COEFFICIENT RAM				CHANNEL 2													
IMF:	6C	FC	85	EE	1A	25	E3	EF	FF	7F	00	00	00	00	00	00	
ECF:	9D	00	F5	FF	1F	FF	9C	04	AD	1A	7C	23	9F	F7	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	8C	FF	6D	FE	8C	42	8C	42	6D	FE	8C	FF	CD	C0	***GTX***	A1	1F
ACR:	E6	00	EA	FC	94	42	94	42	EA	FC	E6	00	01	88	***GRX***	F7	01
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	69	FD	BB	EB	DB	27	FB	EE	FE	7F	00	00	00	00	00	00	
ECF:	BE	01	CD	FE	30	FF	62	02	28	19	76	2C	26	F3	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	C5	FF	CF	FD	01	43	01	43	CF	FD	C5	FF	CD	AC	***GTX***	A1	1F
ACR:	E8	00	92	FC	DC	42	DC	42	92	FC	E8	00	01	88	***GRX***	FD	01
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	2F	FD	EC	EB	2A	28	B5	EE	FF	7F	00	00	00	00	00	00	
ECF:	35	01	70	FF	B0	FF	8C	00	F1	17	41	31	44	F1	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	C3	FF	AB	FD	1A	43	1A	43	AB	FD	C3	FF	CD	AC	***GTX***	A1	1F
ACR:	0C	01	29	FC	1D	43	1D	43	29	FC	0C	01	01	88	***GRX***	FD	01
COEFFICIENT RAM				**CHANNEL 5**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	ED	FF	79	FD	2E	43	2E	43	79	FD	ED	FF	CD	AC	***GTX***	A1	1F
ACR:	1A	01	24	FC	22	43	22	43	24	FC	1A	01	01	88	***GRX***	F1	01
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	B2	FF	64	FD	5A	43	5A	43	64	FD	B2	FF	CD	AC	***GTX***	FF	1F
ACR:	39	01	BC	FB	72	43	72	43	BC	FB	39	01	01	88	***GRX***	F7	01
COEFFICIENT RAM				**CHANNEL 7**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	AB	FF	46	FD	77	43	77	43	46	FD	AB	FF	CD	AC	***GTX***	FF	1F
ACR:	3C	01	66	FB	A9	43	A9	43	66	FB	3C	01	01	88	***GRX***	F7	01
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	01	FB	72	F0	8D	25	F8	EE	FF	7F	00	00	00	00	00	00	
ECF:	BE	FE	D4	02	EB	FF	07	FE	4A	11	CC	41	3B	EA	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	77	FF	32	FD	C1	43	C1	43	32	FD	77	FF	CD	AC	***GTX***	FF	1F
ACR:	2A	01	2C	FB	DE	43	DE	43	2C	FB	2A	01	01	88	***GRX***	FD	01

TABLE 3. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-7.0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

COEFFICIENT RAM				CHANNEL 1													
IMF:	F4	10	83	DB	17	F4	B9	16	41	01	00	00	00	00	00	00	
ECF:	9A	01	C5	FE	EE	FE	C0	03	0D	0C	78	28	D8	F3	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	00	00	BD	FD	FA	42	FA	42	BD	FD	00	00	CD	AC	***GTX***	A1	1F
ACR:	14	01	B8	FC	A2	42	A2	42	B8	FC	14	01	01	88	***GRX***	9F	02
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	92	10	52	DB	5C	F4	DE	16	BF	FF	00	00	00	00	00	00	
ECF:	5B	01	09	FF	3B	FF	65	02	F8	0B	6D	2C	88	F2	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	2E	00	AE	FD	EF	42	EF	42	AE	FD	2E	00	CD	AC	***GTX***	FF	1F
ACR:	2E	01	8F	FC	B9	42	B9	42	8F	FC	2E	01	01	88	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	1D	10	37	DB	A9	F4	F8	16	35	FE	00	00	00	00	00	00	
ECF:	0F	01	5F	FF	8A	FF	44	01	9C	0B	A6	30	09	F1	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	FA	FF	9C	FD	22	43	22	43	9C	FD	FA	FF	CD	AC	***GTX***	FF	1F
ACR:	2A	01	74	FC	D0	42	D0	42	74	FC	2A	01	01	88	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	94	0F	32	DB	FB	F4	07	17	A2	FC	00	00	00	00	00	00	
ECF:	B7	00	C6	FF	CD	FF	67	00	FE	0A	0C	35	5E	EF	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	08	00	73	FD	37	43	37	43	73	FD	08	00	CD	AC	***GTX***	FF	1F
ACR:	41	01	2F	FC	FE	42	FE	42	2F	FC	41	01	01	88	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 5**													
IMF:	55	0F	D9	AF	12	68	95	D8	FF	7F	00	00	00	00	00	00	
ECF:	CE	FE	07	02	13	00	91	FE	C2	09	4E	3C	D5	ED	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	E8	FF	0D	FE	CA	42	CA	42	0D	FE	E8	FF	CD	AC	***GTX***	A1	1F
ACR:	FD	00	FC	FC	74	42	74	42	FC	FC	FD	00	01	99	***GRX***	72	02
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	55	0F	D9	AF	12	68	95	D8	FF	7F	00	00	00	00	00	00	
ECF:	CE	FE	07	02	13	00	91	FE	C2	09	4E	3C	D5	ED	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	E8	FF	0D	FE	CA	42	CA	42	0D	FE	E8	FF	CD	9C	***GTX***	E4	21
ACR:	11	01	BA	FC	A9	42	A9	42	BA	FC	11	01	01	88	***GRX***	90	02

TABLE 3. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-7.0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

COEFFICIENT RAM				CHANNEL 7													
IMF:	54	0F	D8	AF	10	68	94	D8	FC	7F	00	00	00	00	00	00	
ECF:	CC	FE	04	02	10	00	90	FE	C0	09	4C	3C	D4	ED	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	D9	FF	EC	FD	DD	42	DD	42	EC	FD	D9	FF	CD	AC	***GTX***	A1	1F
ACR:	0D	01	9E	FC	BF	42	BF	42	9E	FC	0D	01	01	99	***GRX***	72	02
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	55	0F	D9	AF	12	68	95	D8	FF	7F	00	00	00	00	00	00	
ECF:	CE	FE	07	02	13	00	91	FE	C2	09	4E	3C	D5	ED	00	00	
KM:	00	00	00	00	0	00	00	00	00	00	00	00	00	00	E0	11	
ACT:	D5	FF	CA	FD	FE	42	FE	42	CA	FD	D5	FF	CD	AC	***GTX***	A1	1F
ACR:	05	01	67	FC	EC	42	EC	42	67	FC	05	01	01	99	***GRX***	6B	02

TABLE 4. 200Ω + 680Ω || 0.1µF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB))

COEFFICIENT RAM				CHANNEL 1													
IMF:	E0	12	60	06	E8	E0	18	0C	BC	6A	00	00	00	00	00	00	
ECF:	68	FA	00	0B	FC	FD	D0	1C	C8	E7	D4	4D	70	E3	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	08	07	E4	06	A4	37	A4	37	E4	06	08	07	CC	AC	***GTX***	9E	2A
ACR:	EC	FD	CC	02	38	3F	38	3F	CC	02	EC	FD	00	88	***GRX***	10	04
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	8A	13	BF	06	C7	DE	30	0D	DC	6A	00	00	00	00	00	00	
ECF:	B9	F9	73	0B	03	FF	FB	19	75	E9	43	4F	BD	E2	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	F5	06	D5	06	88	37	88	37	D5	06	F5	06	CD	AC	***GTX***	1C	2B
ACR:	BC	FD	E3	02	27	3F	27	3F	E3	02	BC	FD	01	80	***GRX***	33	04
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	43	14	02	07	AB	DC	4F	0E	EC	6A	00	00	00	00	00	00	
ECF:	24	F9	BC	0B	FC	FF	7D	17	E9	EA	94	50	13	E2	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	EB	06	C3	06	DB	37	DB	37	C3	06	EB	06	CD	AC	***GTX***	E9	2A
ACR:	AC	FD	B8	02	69	3F	69	3F	B8	02	AC	FD	01	88	***GRX***	16	04
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	0F	15	24	07	9A	DA	76	0F	EE	6A	00	00	00	00	00	00	
ECF:	AB	F8	E1	0B	C5	00	83	15	1A	EC	CB	51	72	E1	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	C2	06	78	07	4B	37	4B	37	78	07	C2	06	CD	AC	***GTX***	0F	2B
ACR:	5E	FD	E6	03	92	3E	92	3E	E6	03	5E	FD	01	88	***GRX***	16	04

TABLE 4. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)) (Continued)

COEFFICIENT RAM				CHANNEL 5													
IMF:	F0	15	1C	07	9D	D8	A0	10	E2	6A	00	00	00	00	00	00	
ECF:	52	F8	E2	0B	53	01	18	14	05	ED	EC	52	D7	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	AE	06	B7	07	0E	37	0E	37	B7	07	AE	06	CD	9C	***GTX***	09	2E
ACR:	40	FD	45	04	57	3E	57	3E	45	04	40	FD	01	88	***GRX***	16	04
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	E9	16	E2	06	C0	D6	C8	11	C9	6A	00	00	00	00	00	00	
ECF:	19	F8	B9	0B	A9	01	37	13	AE	ED	FA	53	41	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	B8	06	A4	07	0E	37	0E	37	A4	07	B8	06	CD	AC	***GTX***	36	2B
ACR:	27	FD	6B	04	40	3E	40	3E	6B	04	27	FD	01	88	***GRX***	11	04
COEFFICIENT RAM				**CHANNEL 7**													
IMF:	FC	17	6C	06	0C	D5	E8	12	A0	6A	00	00	00	00	00	00	
ECF:	00	F8	64	0B	CC	01	D0	12	1C	EE	F4	54	AC	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	74	06	18	08	C0	36	C0	36	18	08	74	06	CC	8C	***GTX***	54	31
ACR:	04	FD	B0	04	04	3E	04	3E	B0	04	04	FD	00	88	***GRX***	16	04
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	30	19	B5	05	89	D3	05	14	6F	6A	00	00	00	00	00	00	
ECF:	06	F8	EB	0A	CD	01	D7	12	5B	EE	E3	55	22	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	58	06	6F	08	88	36	88	36	6F	08	58	06	CD	AC	***GTX***	B7	2A
ACR:	AE	FC	74	05	87	3D	87	3D	74	05	AE	FC	01	88	***GRX***	18	04

TABLE 5. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-3.5dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB))

COEFFICIENT RAM				CHANNEL 1													
IMF:	E0	12	60	06	E8	E0	18	0C	BC	6A	00	00	00	00	00	00	
ECF:	68	FA	00	0B	FC	FD	D0	1C	C8	E7	D4	4D	70	E3	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	08	07	E4	06	A4	37	A4	37	E4	06	08	07	CC	AC	***GTX***	9E	2A
ACR:	EC	FD	CC	02	38	3F	38	3F	CC	02	EC	FD	00	88	***GRX***	B7	02
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	8A	13	BF	06	C7	DE	30	0D	DC	6A	00	00	00	00	00	00	
ECF:	B9	F9	73	0B	03	FF	FB	19	75	E9	43	4F	BD	E2	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	F5	06	D5	06	88	37	88	37	D5	06	F5	06	CD	AC	***GTX***	1C	2B
ACR:	BC	FD	E3	02	27	3F	27	3F	E3	02	BC	FD	01	80	***GRX***	CE	02

TABLE 5. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-3.5dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)) (Continued)

COEFFICIENT RAM				CHANNEL 3													
IMF:	43	14	02	07	AB	DC	4F	0E	EC	6A	00	00	00	00	00	00	
ECF:	24	F9	BC	0B	FC	FF	7D	17	E9	EA	94	50	13	E2	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	EB	06	C3	06	DB	37	DB	37	C3	06	EB	06	CD	AC	***GTX***	E9	2A
ACR:	AC	FD	B8	02	69	3F	69	3F	B8	02	AC	FD	01	88	***GRX***	BB	02
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	0F	15	24	07	9A	DA	76	0F	EE	6A	00	00	00	00	00	00	
ECF:	AB	F8	E1	0B	C5	00	83	15	1A	EC	CB	51	72	E1	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	C2	06	78	07	4B	37	4B	37	78	07	C2	06	CD	AC	***GTX***	0F	2B
ACR:	5E	FD	E6	03	92	3E	92	3E	E6	03	5E	FD	01	88	***GRX***	BB	02
COEFFICIENT RAM				**CHANNEL 5**													
IMF:	F0	15	1C	07	9D	D8	A0	10	E2	6A	00	00	00	00	00	00	
ECF:	52	F8	E2	0B	53	01	18	14	05	ED	EC	52	D7	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	AE	06	B7	07	0E	37	0E	37	B7	07	AE	06	CD	9C	***GTX***	09	2E
ACR:	40	FD	45	04	57	3E	57	3E	45	04	40	FD	01	88	***GRX***	BB	02
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	E9	16	E2	06	C0	D6	C8	11	C9	6A	00	00	00	00	00	00	
ECF:	19	F8	B9	0B	A9	01	37	13	AE	ED	FA	53	41	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	B8	06	A4	07	0E	37	0E	37	A4	07	B8	06	CD	AC	***GTX***	36	2B
ACR:	27	FD	6B	04	40	3E	40	3E	6B	04	27	FD	01	88	***GRX***	B3	02
COEFFICIENT RAM				**CHANNEL 7**													
IMF:	FC	17	6C	06	0C	D5	E8	12	A0	6A	00	00	00	00	00	00	
ECF:	00	F8	64	0B	CC	01	D0	12	1C	EE	F4	54	AC	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	74	06	18	08	C0	36	C0	36	18	08	74	06	CC	8C	***GTX***	54	31
ACR:	04	FD	B0	04	04	3E	04	3E	B0	04	04	FD	00	88	***GRX***	BB	02
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	30	19	B5	05	89	D3	05	14	6F	6A	00	00	00	00	00	00	
ECF:	06	F8	EB	0A	CD	01	D7	12	5B	EE	E3	55	22	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	58	06	6F	08	88	36	88	36	6F	08	58	06	CD	AC	***GTX***	B7	2A
ACR:	AE	FC	74	05	87	3D	87	3D	74	05	AE	FC	01	88	***GRX***	BC	02

TABLE 6. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-7.0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

COEFFICIENT RAM				CHANNEL 1													
IMF:	63	F8	2B	4E	47	AF	31	12	3B	6F	00	00	00	00	00	00	
ECF:	15	FD	65	05	22	FF	CE	0E	B2	F3	E3	4D	05	E3	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	E6	06	73	07	55	37	55	37	73	07	E6	06	CD	AC	***GTX***	9E	2A
ACR:	E8	FC	A8	04	21	3E	21	3E	A8	04	E8	FC	01	88	***GRX***	A3	03
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	96	F9	47	4F	77	AA	A7	14	5D	6F	00	00	00	00	00	00	
ECF:	D7	FC	72	05	9E	FF	84	0D	7B	F4	5A	4F	48	E2	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	D4	06	68	07	09	37	09	37	68	07	D4	06	CD	9C	***GTX***	4D	2E
ACR:	BD	FC	D8	04	0D	3E	0D	3E	D8	04	BD	FC	01	88	***GRX***	9A	03
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	F5	FA	01	50	E0	A5	1F	17	74	6F	00	00	00	00	00	00	
ECF:	A4	FC	6E	05	1B	00	5E	0C	2E	F5	B4	50	98	E1	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	F7	06	61	07	50	37	50	37	61	07	F7	06	CD	AC	***GTX***	0F	2B
ACR:	99	FC	1F	05	E5	3D	E5	3D	1F	05	99	FC	01	88	***GRX***	A0	03
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	84	FC	4F	50	8F	A1	93	19	80	6F	00	00	00	00	00	00	
ECF:	7D	FC	5C	05	82	00	73	0B	C1	F5	F1	51	F2	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	D3	06	B6	07	1D	37	1D	37	B6	07	D3	06	CD	AC	***GTX***	0F	2B
ACR:	92	FC	6D	05	A2	3D	A2	3D	6D	05	92	FC	01	88	***GRX***	9B	03
COEFFICIENT RAM				**CHANNEL 5**													
IMF:	44	FE	27	50	91	9D	FD	1B	80	6F	00	00	00	00	00	00	
ECF:	62	FC	3D	05	CB	00	CB	0A	33	F6	17	53	53	E0	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	CD	06	C9	07	FC	36	FC	36	C9	07	CD	06	CD	AC	***GTX***	DD	2A
ACR:	6E	FC	B3	05	7A	3D	7A	3D	B3	05	6E	FC	01	88	***GRX***	A1	03
COEFFICIENT RAM				**CHANNEL 6**													
IMF:	3A	00	7D	4F	F5	99	56	1E	74	6F	00	00	00	00	00	00	
ECF:	55	FC	10	05	F6	00	66	0A	86	F6	28	54	BB	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	C6	06	DA	07	CB	36	CB	36	DA	07	C6	06	CD	9C	***GTX***	5A	2E
ACR:	32	FC	1F	06	3D	3D	3D	3D	1F	06	32	FC	01	88	***GRX***	94	03

TABLE 6. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-7.0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

COEFFICIENT RAM				CHANNEL 7													
IMF:	68	02	48	4E	C6	96	9A	20	5D	6F	00	00	00	00	00	00	
ECF:	56	FC	D4	04	06	01	3F	0A	BB	F6	25	55	29	DF	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	CB	06	D8	07	B6	36	B6	36	D8	07	CB	06	CD	9C	***GTX***	31	2E
ACR:	5C	FC	EF	05	51	3D	51	3D	EF	05	5C	FC	01	88	***GRX***	9C	03
COEFFICIENT RAM				**CHANNEL 8**													
IMF:	D0	04	83	4C	0E	94	C5	22	39	6F	00	00	00	00	00	00	
ECF:	63	FC	87	04	00	01	4B	0A	D9	F6	12	56	9C	DE	00	00	
KM:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	40	E0	
ACT:	8A	06	6B	08	7D	36	76	36	6B	08	8A	06	CD	9C	***GTX***	EE	2D
ACR:	2E	FC	86	06	EF	3C	EF	3C	86	06	2E	FC	01	88	***GRX***	98	03

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE
Intersil Europe Sarl
Ave. William Graisse, 3
1006 Lausanne
Switzerland
TEL: +41 21 6140560
FAX: +41 21 6140579

ASIA
Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433